AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Original) The method of claim 1,

wherein the adjusting step comprises subtracting the error signal corresponding to each crest from the input signal,

wherein the forming step comprises the step of filtering the error signal to conform with an out-of-band transmission specification, and

wherein the forming and adjusting steps are implemented at a sampling rate of at least four times the chip rate, and

wherein the method further comprises the step of power-amplifying an outcome of the subtracting step.

9. (Original) A method of reducing a peak-to-average ratio of an input signal, comprising the steps of:

forming an error signal that corresponds to crests of the input signal, wherein, when a given crest of the input signal corresponds to more than one sample of the input signal, the error signal is substantially independent of samples that do not correspond to a maximum amplitude of the crest; and

adjusting the input signal based on the error signal.

10. (Original) The method of claim 9, further comprising the step of power-amplifying an outcome of the adjusting step.

11. (Original) The method of claim 9, wherein the adjusting step comprises subtracting the error signal corresponding to each crest from the input signal.

12. (Original) The method of claim 11, wherein the error signal is subtracted from a delayed version of the input signal.

13. (Original) The method of claim 9, wherein the forming step comprises the step of filtering the error signal to conform with an out-of-band transmission specification.

14. (Original) The method of claim 9, further comprising the steps of repeating the forming and adjusting steps on an outcome of the adjusting step.

15. (Original) The method of claim 9, wherein the forming and adjusting step are implemented at a sampling rate of at least four times the chip rate.

16. (Original) The method of claim 9,

wherein the adjusting step comprises subtracting the error signal corresponding to each crest from the input signal,

wherein the forming step comprises the step of filtering the error signal to conform with an out-of-band transmission specification, and

wherein the forming and adjusting steps are implemented at a sampling rate of at least four times the chip rate, and

wherein the method further comprises the step of power-amplifying an outcome of the subtracting step.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Original) A method of reducing a peak-to-average ratio of an input signal, comprising the steps of:

detecting short crests of the input signal that correspond to only one sample of the input signal;

detecting long crests of the input signal that correspond to more than one sample of the input signal;

selecting, for each detected long crest, respectively, a sample of the input signal having a maximum amplitude;

decresting each of the short crests, respectively, based on the sample of the input signal that corresponds to the respective short crest; and

decresting each of the long crests, respectively, based on the sample selected in the selecting step for the respective long crest.

26. (Original) The method of claim 25, further comprising the step of power-amplifying an outcome of the decresting step.

27. (Original) The method of claim 25, wherein each decresting step comprises the step of subtracting a signal corresponding to each crest from the input signal.

28. (Original) The method of claim 27, wherein each decresting step further comprises the step of filtering the signal corresponding to each crest to conform with an out-of-band transmission specification prior to implementing the subtracting step.

29. (Original) The method of claim 25, further comprising the steps of repeating the detecting, selecting, and decresting steps on an outcome of each decresting step.

30. (Original) The method of claim 29, further comprising the step of power-amplifying an outcome of the repeating steps.

31. (Original) The method of claim 25, wherein the detecting, selecting, and decresting steps are implemented at a sampling rate of at least four times the chip rate.

32. (Currently amended) A signal amplification system, comprising:

a peak power factor reducer including a first local peak detector, a first decrester coupled with said first local peak detector, and a second decrester coupled to said first decrester.

33. (Canceled)

34. (Canceled)

35. (Currently amended) The system of claim ~~34~~ 32, further including a second local peak detector coupled to said second decrester.

36. (Original) The system of claim 35, wherein said first local peak detector selects a first sample value from among a first group of sample values, said first sample having the highest amplitude among said first group of sample values.

37. (Original) The system of claim 36, wherein said second local peak detector selects a second sample value from among a second group of sample values, said sample having the highest amplitude among said second group of sample values.

38. (Original) The system of claim 37, wherein said first decrester includes:

a first rectangular to polar converter having first inphase (I) and first quadrature (Q) signal inputs coupled to a first input signal and a first amplitude (A) output and first phase (Φ) output signal, an input of said first local peak detector coupled to said A output;

a first amplitude threshold discriminator including a first local peak input (A'), a first threshold (Th) input, and a first error output (E), said A' input coupled to an output of said first peak detector;

a first threshold generator coupled to the first Th input of said first amplitude threshold discriminator, said first threshold generator providing a first threshold value to said first amplitude threshold discriminator;

a first multiplier coupled to said first error output and said first phase signal, said first multiplier multiplying said first error output signal by said first phase signal;

a first error filter coupled to said first multiplier and receiving said phase adjusted error signal and generating a first filtered error signal from said first multiplier; and

a first subtractor coupled to said first filtered error signal and a delayed first input signal, said first subtractor outputting a first stage decrested signal.

39. (Original) The system of claim 38, wherein said second decrester includes:

a second rectangular to polar converter having second inphase (I) and second quadrature (Q) signal inputs coupled to said first stage decrested signal and a second amplitude

(A) output and second phase (Φ) output signal, an input of said second local peak detector coupled to said A output;

a second amplitude threshold discriminator including a second local peak input (A'), a second threshold (Th) input, and a second error output (E), said A' input coupled to an output of said second peak detector;

a second threshold generator coupled to the second Th input of said second amplitude threshold discriminator, said second threshold generator providing a second threshold value to said second amplitude threshold discriminator;

a second multiplier coupled to said second error output and said second phase signal, said second multiplier multiplying said second error output signal by said second phase signal;

a second error filter coupled to said second multiplier and receiving said phase adjusted error signal and generating a second filtered error signal from said second multiplier; and

a second subtractor coupled to said second filtered error signal and a delayed second input signal, said second subtractor outputting a second stage decrested signal.

40. (Original) The system of claim 39, wherein said first input signal has a high peak-to-average power ratio, the first amplitude threshold and the second amplitude threshold are the same, and the first decrester is cascaded with the second decrester.

41. (Original) The system of claim 40, wherein said first input signal is a code division multiple access (CDMA) signal and the peak power factor reducer operates at a sample rate of four times a chip rate.

42. (Currently amended) A base station, comprising:

a power amplifier; and

a peak power factor reducer coupled to said power amplifier, said peak power factor reducer including a first local peak detector to improve said power amplifier efficiency, a first decrester coupled with said first local peak detector, and a second decrester coupled to said first decrester.

43. (Canceled)

44. (Canceled)

45. (Currently amended) The system of claim 44 42, further including a second local peak detector coupled to said second decrester.

46. (Original) The system of claim 45, wherein said first local peak detector selects a first sample value from among a first group of sample values, said first sample having the highest amplitude among said first group of sample values.

47. (Original) The system of claim 46, wherein said second local peak detector selects a second sample value from among a second group of sample values, said sample having the highest amplitude among said second group of sample values.

48. (Original) The system of claim 47, wherein said first decrester includes:

a first rectangular to polar converter having first inphase (I) and first quadrature (Q) signal inputs coupled to a first input signal and a first amplitude (A) output and first phase (Φ) output signal, an input of said first local peak detector coupled to said A output;

a first amplitude threshold discriminator including a first local peak input (A'), a first threshold (Th) input, and a first error output (E), said A' input coupled to an output of said first peak detector;

a first threshold generator coupled to the first Th input of said first amplitude threshold discriminator, said first threshold generator providing a first threshold value to said first amplitude threshold discriminator;

a first multiplier coupled to said first error output and said first phase signal, said first multiplier multiplying said first error output signal by said first phase signal;

a first error filter coupled to said first multiplier and receiving said phase adjusted error signal and generating a first filtered error signal from said first multiplier; and

a first subtractor coupled to said first filtered error signal and a delayed first input signal, said first subtractor outputting a first stage decrested signal.

49. (Original) The system of claim 48, wherein said second decrester includes:

a second rectangular to polar converter having second inphase (I) and second quadrature (Q) signal inputs coupled to said first stage decrested signal and a second amplitude (A) output and second phase (Φ) output signal, an input of said second local peak detector coupled to said A output;

a second amplitude threshold discriminator including a second local peak input (A'), a second threshold (Th) input, and a second error output (E), said A' input coupled to an output of said second peak detector;

a second threshold generator coupled to the second Th input of said second amplitude threshold discriminator, said second threshold generator providing a second threshold value to said second amplitude threshold discriminator;

a second multiplier coupled to said second error output and said second phase signal, said second multiplier multiplying said second error output signal by said second phase signal;

a second error filter coupled to said second multiplier and receiving said phase adjusted error signal and generating a second filtered error signal from said second multiplier; and

a second subtractor coupled to said second filtered error signal and a delayed second input signal, said second subtractor outputting a second stage decrested signal.

50. (Original) The system of claim 49, wherein said first input signal has a high peak-to-average power ratio, the first amplitude threshold and the second amplitude threshold are the same, and the first decrester is cascaded with the second decrester.

51. (Original) The system of claim 50, wherein said first input signal is a code division multiple access (CDMA) signal and the peak power factor reducer operates at a sample rate of four times a chip rate.

52. (Currently Amended) A method for improving the efficiency of an amplifier, comprising the steps of:

detecting a first maximum signal amplitude sample value from a first group of signal amplitude sample values derived from ~~a~~ an input signal;

generating a first error signal based on said first maximum signal amplitude sample value while eliminating other signal amplitude sample values of said first group of signal amplitude sample values; ~~and~~

decresting said first input signal with said first error signal so as to reduce overshoot and undershoot of said decresting that occurs due to quick variations in several signal amplitude sample values of said first group of signal amplitude sample values;

detecting a second maximum signal amplitude sample value from a second group of signal amplitude sample values derived from a previously decrested signal;

generating a second error signal based on said second maximum signal amplitude sample value while eliminating other signal amplitude sample values of said second group of signal amplitude sample values; and

decresting said second input signal with said second error signal so as to reduce overshoot and undershoot of said decresting that occurs due to quick variations in several signal amplitude sample values of said second group of signal amplitude sample values.

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53. (Canceled)

54. (Currently amended) The method of claim ~~53~~ 52, wherein the input signal has a high peak-to-average power ratio and said peak-to-average power ratio is reduced.

55. (Original) The method of claim 54, wherein said input signal is a code division multiple access (CDMA) signal.

56. (Original) The method of claim 55, wherein said amplifier operates closer to saturation and less signal information is eliminated.